AMENDMENTS TO THE CLAIMS:

Please cancel claims 6–7, 17 and 20 without prejudice. Please amend the remaining claims as follows, substituting any amended claim(s) for the corresponding pending claim(s):

1. (Currently Amended) A microprocessor comprising:

a first integrated circuit chip having an active face including a central processing unit; and

a second integrated circuit chip mounted on, and electrically connected to, the active face of the first integrated circuit, wherein the second integrated circuit chip provides added functionality to the central processing unit of the first integrated circuit,

wherein at least one metal region projecting from the active face of the first integrated circuit chip overlies at least one metal region projecting from a surface of the second integrated circuit chip, and

wherein the second integrated circuit chip is spaced apart from the first integrated chip by a distance of at least a projection height of the at least one metal region projecting from the active face of the first integrated circuit chip plus a projection height of the at least one metal region projecting from the surface of the second integrated circuit chip, wherein the distance is sufficient to permit electrical connection to contact pads on the active surface of the first integrated circuit chip for external connection to the central processing unit.

2. (Previously Presented) The microprocessor of claim 1, wherein the central processing unit comprises one of a digital signal processor and a field programmable gate array.

3. (Previously Presented) The microprocessor of claim 1, wherein an active face of the second integrated circuit chip faces the active face of the first integrated circuit chip.

4. (Previously Presented) The microprocessor of claim 1, wherein the second integrated circuit chip comprises one of a memory and an analog-to-digital converter.

5. (Previously Presented) The microprocessor of claim 4, wherein the second integrated circuit comprises one of a cache memory, a dynamic random access memory (DRAM), a static random access memory (SRAM), and a flash memory.

Claims 6–7 (Canceled)

8. (Currently Amended) The microprocessor of claim ~~6~~ 1, further comprising:

a bonding layer between and electrically connecting the at least one metal region projecting from the active face of the first integrated circuit chip and the at least one metal region projecting from a surface of the second integrated circuit chip, wherein the bonding layer provides mechanical bonding of the first and second integrated circuit chips.

9. (Previously Presented) The microprocessor of claim 1, further comprising:

at least two groups of contact pads on the active surface of the first integrated circuit chip for external connection to the central processing unit, wherein the second integrated circuit chip has a width less than a distance between the two groups of contact pads.

10. (Previously Presented) The microprocessor of claim 1, further comprising:

a third integrated circuit chip mounted on, and electrically connected to, the active face of the first integrated circuit adjacent the second integrated circuit chip, wherein the third integrated circuit chip adds further functionality to the central processing unit of the first integrated circuit.

11. (Previously Presented) The microprocessor of claim 1, wherein the electrical connection between the first integrated circuit chip and the second integrated circuit chip is by direct connection of metal regions on the active faces of the first and second integrated circuit chips by a bonding layer.

12. (Previously Presented) The microprocessor of claim 1, wherein a length and width of the second integrated circuit chip are less than a respective length and width of the first integrated circuit chip.

13. (Currently Amended) A microprocessor comprising:

a first chip having an active face including a central processing unit; and

a second chip having an active face, the second chip mounted on, and electrically connected to, the active face of the first chip, wherein the second chip adds functionality to the central processing unit of the first chip and wherein the electrical connection is by a bonding layer between metal regions on the active faces of the first and second chips, and wherein at least one of the metal regions on the active surface of the first chip is disposed over a portion of an integrated circuit forming the central processing unit.

14. (Previously Presented) The microprocessor of claim 13, wherein the metal regions further comprise one of:

conductive regions projecting from the active faces of the first and second chips; and

conductive layers over insulating regions projecting from the active faces of the first and second chips,

wherein the active regions of the first and second chips are spaced apart by the metal regions.

15. (Previously Presented) The microprocessor of claim 13, wherein the central processing unit comprises one of a digital signal processor and a field programmable gate array.

16. (Previously Presented) The microprocessor of claim 13, wherein the second chip comprises one of a memory and an analog-to-digital converter.

Claim 17. (Canceled)

18. (Previously Presented) The microprocessor of claim 13, further comprising:

a third chip mounted on, and electrically connected to, the active face of the first chip adjacent the second chip wherein the third chip adds further functionality to the central processing unit of the first chip.

19. (Previously Presented) The microprocessor of claim 13, wherein a width of the second integrated circuit chip is less than a width of the first integrated circuit chip.

20. (Canceled).